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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,304	12/03/2003	Chien-Te Chen	60417 (71987)	9698

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EXAMINER

NGUYEN, TUNG X

ART UNIT	PAPER NUMBER
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2829

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/728,304

Applicant(s)

CHEN ET AL.

Examiner

Tung X. Nguyen

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-7 are rejected under 35 U.S.C. 102(a) as being anticipated by Ogawa et al. (u.s.p 6,577,490).

As to claim 1, Ogawa et al. disclose in Figs. 1-16, a chip carrier comprising: a core layer (122 of figure 16) having a plurality of conductive traces (125-126, 945 of figure 16) formed on at least one surface; the conductive traces (125 of figure 16) comprising:

At least one first trace (126 of figure 16) connected with the passive component (160 of figure 16) and having a first predetermined position (under 122) and two ends (126 connecting to 128 and 912 of figure 16); wherein the two ends are respectively electrically connected to a first bond finger (first end of 126 connect to 128 of figure 16) formed on the surface, mounted with the passive component (160); and to a first ball pad (949 of figure 16) formed on an opposite surface of the chip carrier (901 of figure 16); wherein the first predetermined position and the first bond finger are located on the same side relative to the passive component (fig. 16); and

At least one second trace (trace connecting to 927 of figure 16) free of connection with the passive component (160 of figure 16) and having two ends and a

second predetermined position (under 930 of figure 16) located on the same surface as the first predetermined position; wherein one of the ends of the second trace is electrically connected to a second ball pad (927) located on the same surface as the first ball pad (949 of figure 16); and

A solder mask layer (121-122 of figure 16) applied over the conductive traces and formed with a plurality of openings (129) for at least exposing the first predetermined position and the second predetermined position.

As to claims 2-3, Ogawa et al. discloses in Figs. 1-16, the passive component (160 of figure 16) is a resistor or inductor (160).

As to claim 4, Ogawa et al. disclose (col. 11, lines 20-25) each of the first predetermined position and the second predetermined position is at least formed with a nickel/gold (Ni/Au) layer.

As to claim 5, Ogawa et al. discloses the chip carrier (900 of figure 16) is a substrate (901 of figure 16).

As to claim 6, Ogawa et al. discloses the chip carrier, wherein the passive component (160 of figure 16) is serially connected to the first trace by means of surface mount technology (SMT).

As to claim 7, Ogawa et al. discloses the core layer (col. 2, lines 57-65) is made of a material selected from the group consisting of FR4 resin, glass resin, BT (bismaleimide triazine) resin, epoxy resin, polyimide resin, and cyanide resin.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 8, 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. (u.s.p 6,577,490), in view of Admitted Prior Art (heretoafter APA).

As to claim 8, Ogawa et al. disclose in Figs. 1-16, a chip carrier comprising: a core layer (122 of figure 16) having a plurality of conductive traces (125-126, 945 of figure 16) formed on at least one surface; the conductive traces (125 of figure 16) comprising:

At least one first trace (126 of figure 16) connected with the passive component (160 of figure 16) and having a first predetermined position (under 122) and two ends (126 connecting to 128 and 912 of figure 16); wherein the two ends are respectively electrically connected to a first bond finger (first end of 126 connect to 128 of figure 16) formed on the surface, mounted with the passive component (160); and to a first ball pad (949 of figure 16) formed on an opposite surface of the chip carrier (901 of figure 16); wherein the first predetermined position and the first bond finger are located on the same side relative to the passive component (fig. 16); and

At least one second trace (trace connecting to 927 of figure 16) free of connection with the passive component (160 of figure 16) and having two ends and a second predetermined position (under 930 of figure 16) located on the same surface as

the first predetermined position; wherein one of the ends of the second trace is electrically connected to a second ball pad (927) located on the same surface as the first ball pad (949 of figure 16); and

A solder mask layer (121-122 of figure 16) applied over the conductive traces and formed with a plurality of openings (129) for at least exposing the first predetermined position and the second predetermined position.

Ogawa et al. Do not disclose the two test heads respectively with the first ball pad and second ball pad, which are situated on the same surface of the chip carrier, to testing the electrical performance of the passive component.

However, APA disclose in Figs. two test heads respectively with the first ball pad (87 of figure 8) and second ball pad (85 of figure 8), which are situated on the same surface of the chip carrier, to testing the electrical performance of the passive component (81) for transmitting signal from the passive component to the tester. Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Ogawa et al. and provide the two test head, as taught by APA for transmitting signal from the passive component to the tester.

As to claims 11-12, Ogawa et al. discloses in Figs. 1-16, the passive component (160 of figure 16) is a resistor or inductor (160).

As to claim 13, Ogawa et al. disclose (col. 11, lines 20-25) each of the first predetermined position and the second predetermined position is at least formed with a nickel/gold (Ni/Au) layer.

As to claim 14, Ogawa et al. discloses the chip carrier (900 of figure 16) is a substrate (901 of figure 16).

As to claim 15, Ogawa et al. discloses the chip carrier, wherein the passive component (160 of figure 16) is serially connected to the first trace by means of surface mount technology (SMT).

As to claim 16, Ogawa et al. discloses the core layer (col. 2, lines 57-65) is made of a material selected from the group consisting of FR4 resin, glass resin, BT (bismaleimide triazine) resin, epoxy resin, polyimide resin, and cyanide resin.

As to claim 17, Ogawa et al. discloses all of the limitation except for the test head is a test probe (61 of figure 8) of a test system. However, APA disclose the test head (80 of figure 8) is a test probe (61 of figure 8) of a test system for transmitting the signal from the passive component to the tester. Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to of Ogawa et al., and provide the test head with a test probe, as taught by APA for transmitting the signal from the passive component to the tester.

5. Claims 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. (u.s.p 6,577,490), in view of Pedersen et al. (u.s.p 5,698,895).

As to claims 9-10, Ogawa et al. discloses all of the limitations except for the conductive jig made by conductive rubber or metal. However, Pedersen et al. disclose the conductive jig consider to be conductive fuse (50a of figure 2) for enabling the passive component tested on the same time (col. 10, lines 1-10). Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention

was made to modify the system of Ogawa et al., and provides the conductive jig, as taught by Pedersen et al. for enabling the passive component tested on the same time (col. 10, lines 1-10).

### ***Response to Arguments***

6. Applicant's arguments, see Remark on pages 3-5, filed 4/1/05, with respect to claims 1-17 have been fully considered and are persuasive. The last Office Action has been withdrawn.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X. Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN  
6/22/05

  
VINH NGUYEN  
PRIMARY EXAMINER  
A.U. 2829  
06/23/05